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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,896	JAIN ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 19, 2004.*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated October 19, 2004. Claims 1, 5, 6, 11, 13, 15 and 16 were amended. Claims 1-17 of the application are pending and rejected. This office action is made final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 4-6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Swoboda et al.** (U.S. Patent 6,704,895).

4.1 **Matsumura et al.** teaches Semiconductor integrated circuit design and evaluation system using cycle-base timing. Specifically, as per claim 1, **Matsumura et al.** teaches a method of evaluating performance of a test environment and an actual electronic device during testing of the electronic device (CL1, L10-17; CL2, L39-46); the method comprising:

creating a virtual test environment emulating an actual test environment in which the actual electronic device is to be tested (CL1, L10-17; CL2, L39-46; Fig 2, Item 11; CL5, L41-53);

implanting a virtual device emulating the actual electronic device into the virtual test environment (Fig 2, Item 45; Abstract,, L6-8; Fig 1, Item 13_2; CL2, L42-46; CL3, L23-28); and

stimulating the virtual device with an input test signal emulating an actual input signal to be applied to the actual electronic device during testing (Fig 1, Input to Item 11; Fig 2, Item 28; Fig 1, Item 13_1; CL2, L42-46).

Matsumura et al. does not expressly teach that the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches that the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow testing the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of

Matsumura et al. with the method of **Swoboda et al.** that included the actual test environment being meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow testing the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner.

Matsumura et al. does not expressly teach determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment. **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Matsumura et al.** with the method of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner; allow simulating the

target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Matsumura et al. does not expressly teach determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Matsumura et al.** with the method of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a

cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Matsumura et al. teaches evaluating the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54). **Matsumura et al.** does not expressly teach evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment; and determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target

device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Matsumura et al.** with the method of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment; and determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used, so that would allow evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Per claim 4: **Matsumura et al.** teaches performing a virtual adjustment of the virtual device based on the evaluation (CL3, L1-10).

Per claim 5: **Matsumura et al.** teaches improving the design of the actual electronic device based on the evaluation (CL3, L1-10).

4.2 As per claim 6, **Matsumura et al.** teaches an article, comprising a storage medium having instructions stored thereon, the instructions when executed evaluating performance of a test environment and of an actual electronic device during testing of the actual electronic device (Abstract, L1-21; Fig 1; CL4, L24-29; CL1, L10-17; CL2, L39-46);

creating a virtual test environment emulating an actual test environment in which the electronic device is to be tested (CL1, L10-17; CL2, L39-46; Fig 2, Item 11; CL5, L41-53);

implanting a virtual device emulating the actual electronic device into the virtual test environment (Fig 2, Item 45; Abstract,, L6-8; Fig 1, Item 13_2; CL2, L42-46; CL3, L23-28); and

stimulating the virtual device with an input test signal emulating an actual input signal to be applied to the actual electronic device during testing (Fig 1, Input to Item 11; Fig 2, Item 28; Fig 1, Item 13_1; CL2, L42-46).

Matsumura et al. does not expressly teach that the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches that the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow testing the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the storage medium having instructions of **Matsumura et al.** with the storage medium having instructions of

Swoboda et al. that included the actual test environment being meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow testing the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner.

Matsumura et al. does not expressly teach determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment. **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the storage medium having instructions of **Matsumura et al.** with the storage medium having instructions of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes

them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Matsumura et al. does not expressly teach determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the storage medium having instructions of **Matsumura et al.** with the storage medium having instructions of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow

simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Matsumura et al. teaches evaluating the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54). **Matsumura et al.** does not expressly teach evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment; and determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by

one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the storage medium having instructions of **Matsumura et al.** with the storage medium having instructions of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment; and determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used, so that would allow evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Per claim 9: **Matsumura et al.** teaches the instructions when executed additionally perform a virtual adjustment of the virtual device based on the evaluation (CL3, L1-10).

Per claim 10: **Matsumura et al.** teaches the instructions when executed additionally improve the design of the actual device based on the evaluation (CL3, L1-10).

5. Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Swoboda et al.** (U.S. Patent 6,704,895), and further in view of **Dang** (U.S. Patent 5,931,962).

5.1 As per claims 2 and 3, **Matsumura et al.** and **Swoboda et al.** teach the method of claim 1. **Matsumura et al.** teaches that the LSI tester simulator compares the output signals from the logic simulator (virtual device) with the expected data to determine the correctness of the test pattern (that includes the test environment correctness) or performances of the LSI device (CL3, L6-10).

Matsumura et al. does not expressly teach performing a virtual calibration of the virtual test environment; and improving the virtual calibration based on the evaluation. **Dang** teaches performing a virtual calibration of the virtual test environment; and improving the virtual calibration based on the evaluation (CL2, L35-37), because that will compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry (CL2, L17-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Matsumura et al.** with the method of **Dang** that included performing a virtual calibration of the virtual test environment; and improving the virtual calibration based on the

evaluation. The artisan would have been motivated because that would compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry.

5.2 As per claims 7 and 8, **Matsumura et al.** and **Swoboda et al.** teach the article of claim 6. **Matsumura et al.** teaches a storage medium having instructions stored thereon for the LSI tester simulator to compare the output signals from the logic simulator (virtual device) with the expected data to determine the correctness of the test pattern (that includes the test environment correctness) or performances of the LSI device (CL3, L6-10).

Matsumura et al. does not expressly teach that the instructions when executed additionally perform a virtual calibration of the virtual test environment; and the instructions when executed additionally improve the virtual calibration based on the evaluation. **Dang** teaches that the instructions when executed additionally perform a virtual calibration of the virtual test environment; and the instructions when executed additionally improve the virtual calibration based on the evaluation (CL2, L35-37), because that will compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry (CL2, L17-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the storage medium having instructions of **Matsumura et al.** with the storage medium having instructions of **Dang** that included the instructions that when executed additionally performed a virtual calibration of the virtual test environment; and the instructions when executed

additionally improved the virtual calibration based on the evaluation. The artisan would have been motivated because that would compensate for timing inaccuracies due to unequal electrical cable length and non-linear response of the testing circuitry and errors in modeling of the testing circuitry.

6. Claims 11-13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Swoboda et al.** (U.S. Patent 6,704,895), and further in view of **Tuan et al.** (U.S. Patent 5,872,952), and **Panis** (U.S. Patent 6,550,036).

6.1 As per claim 11, **Matsumura et al.** teaches an apparatus for evaluating the performance of a test environment and of an actual electronic device (Abstract, L1-21; Fig 1; CL4, L24-29; CL1, L10-17; CL2, L39-46); the apparatus comprising:

a virtual device emulating the actual electronic device (Fig 2, Item 45; Abstract,, L6-8; Fig 1, Item 13_2; CL2, L42-46; CL3, L23-28); and

a virtual test environment emulating an actual test environment in which the actual electronic device is to be tested (CL1, L10-17; CL2, L39-46; Fig 2, Item 11; CL5, L41-53); to apply to the virtual device an input test signal emulating an actual input signal to be applied to the actual electronic device during testing (Fig 1, Input to Item 11; Fig 2, Item 28; Fig 1, Item 13_1; CL2, L42-46).

Matsumura et al. does not expressly teach that the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might

ordinarily be used. **Swoboda et al.** teaches that the actual test environment is meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow testing the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Swoboda et al.** that included the actual test environment being meant to emulate the actual electronic device in an environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow testing the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner.

Matsumura et al. teaches circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54). **Matsumura et al.** does not expressly teach to determine an indication of a signal transmission time of the actual electronic device in the actual test environment and to determine an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. **Swoboda et al.** teaches to determine an indication of a signal transmission time of the actual electronic device in the actual test environment and to determine an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a

cost-effective manner (CL6, L26-28); allow simulating the target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Swoboda et al.** that included to determine an indication of a signal transmission time of the actual electronic device in the actual test environment and to determine an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Matsumura et al. does not expressly teach virtual timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device. **Tuan et al.** teaches virtual timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (CL10, L21-26; CL10, L60 to CL11, L10), because as per **Panis** the timing circuitry will provide timing relationships of the device under test to measurement instrument (timer) which measures the time intervals between the signals (CL2,

L47-48; CL1, L28-30). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Tuan et al.** that included virtual timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device. The artisan would have been motivated because the timing circuitry would provide timing relationships of the device under test to measurement instrument (timer) which would measure the time intervals between the signals.

Matsumura et al. teaches circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (Fig 2, Item 27; CL3, L30-33; CL5, L47-54). **Tuan et al.** teaches virtual timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (CL10, L21-26; CL10, L60 to CL11, L10). **Matsumura et al.** does not expressly teach the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used are used to evaluate the integrity of the input test signal and a resulting output signal from the virtual device. **Swoboda et al.** teaches the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used are used to evaluate the integrity of the input test signal and a resulting output signal from the virtual device (CL6, L26-31; CL12, L45-57; CL44, L10-19), because that will allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner (CL6, L26-28); allow simulating the

target device even when the rest of the circuitry for the target board is incomplete (CL12, L49-51); and allows simulating the target board and the target device, so that software development for the device can be performed by one group of engineers while another group of engineers is designing as yet unfinished target device and system (CL44, L11-14). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Swoboda et al.** that included the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used are used to evaluate the integrity of the input test signal and a resulting output signal from the virtual device. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port when the target chip includes them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Per claim 12: **Matsumura et al.** teaches the virtual test environment emulates a general purpose tester and a tester interface unit specific to the electronic device (Abstract, L1-21; Fig 1; CL4, L24-29).

6.2 As per claim 13, **Matsumura et al., Swoboda et al., Tuan et al.** and **Panis** teach the apparatus of claim 12. **Matsumura et al.** does not expressly teach that the virtual timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. **Tuan et al.** teaches that the virtual timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device (CL10, L21-26; CL10, L60 to CL11, L10), because as per **Panis** that allows accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products have time critical specifications (CL2, L40-41; CL1, L28-30; CL1, L10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Tuan et al.** that included the virtual timing circuitry comprising a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. The artisan would have been motivated because that would allow accurate and easy measurement of time intervals

between first and second signal edges designated as start and stop events because many electronic products would have time critical specifications.

6.3 As per claim 16, **Matsumura et al., Swoboda et al., Tuan et al.** and **Panis** teach the apparatus of claim 11. **Matsumura et al.** does not expressly teach that the virtual timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. **Tuan et al.** teaches that the virtual timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device (CL10, L21-26; CL10, L60 to CL11, L10), because as per **Panis** that allows accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products have time critical specifications (CL2, L40-41; CL1, L28-30; CL1, L10). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Tuan et al.** that included the virtual timing circuitry comprising a first timer to determine the time interval between output of the input test signal by the virtual test environment and receipt of the output test signal by the virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by the

virtual device and output of the output test signal by the virtual device. The artisan would have been motivated because that would allow accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products would have time critical specifications.

Per claim 17: **Matsumura et al.** teaches the apparatus comprising a general purpose processing system (Abstract, L1-21; Fig 1; CL4, L24-29).

7. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (U.S. Patent 6,370,675) in view of **Swoboda et al.** (U.S. Patent 6,704,895), and further in view of **Tuan et al.**(U.S. Patent 5,872,952), **Panis** (U.S. Patent 6,550,036) and **Dang** (U.S. Patent 5,931,962).

7.1 As per claim 14, **Matsumura et al., Swoboda et al., Tuan et al.** and **Panis** teach the apparatus of claim 11. **Matsumura et al.** does not expressly teach that the virtual test environment comprises a virtual test driver to apply the input test signal to the virtual device, and a virtual test receiver to receive the output test signal from the virtual device. **Dang** teaches that the virtual test environment comprises a virtual test driver to apply the input test signal to the virtual device, and a virtual test receiver to receive the output test signal from the virtual device (CL5, L33-48), because the test driver contains the pin electronics for driving the test signal to the device under test and the test receiver contains pin electronics to receive signals from the device under test in response to the test signals (CL5, L43-45). It would have been obvious to

one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Dang** that included the virtual test environment comprising a virtual test driver to apply the input test signal to the virtual device, and a virtual test receiver to receive the output test signal from the virtual device. The artisan would have been motivated because the test driver would contain the pin electronics for driving the test signal to the device under test and the test receiver would contain pin electronics to receive signals from the device under test in response to the test signals.

7.2 As per claim 15, **Matsumura et al., Swoboda et al., Tuan et al., Panis** and **Dang** teach the apparatus of claim 14. **Matsumura et al.** does not expressly teach that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test driver and receipt of the output test signal by the virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. **Tuan et al.** teaches that the timing circuitry comprises a first timer to determine the time interval between output of the input test signal by the virtual test driver and receipt of the output test signal by the virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device (CL10, L21-26; CL10, L60 to CL11, L10), because as per **Panis** that allows accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products have time critical specifications (CL2, L40-41; CL1, L28-30; CL1, L10). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the apparatus of **Matsumura et al.** with the apparatus of **Tuan et al.** that included the timing circuitry comprising a first timer to determine the time interval between output of the input test signal by the virtual test driver and receipt of the output test signal by the virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by the virtual device and output of the output test signal by the virtual device. The artisan would have been motivated because that would allow accurate and easy measurement of time intervals between first and second signal edges designated as start and stop events because many electronic products would have time critical specifications.

Response to Arguments

8. Applicant's arguments filed on October 19, 2004 have been fully considered. The arguments with respect to 103 (a) rejections are not persuasive.

8.1 As per the applicants' argument that "independent claims 1, 6 and 11 have been amended to include similar features of determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment; determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used; and evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission

time of the actual electronic device in the environment the actual electronic device might ordinarily be used; the Matsumura, Dang and/or Panis patents, either taken alone or in combination, do not teach or suggest the above added features", the examiner has used new reference **Swoboda et al.**

Swoboda et al. teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment (CL6, L26-31; CL12, L45-57; CL44, L10-19). **Swoboda et al.** teaches determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used (CL6, L26-31; CL12, L45-57; CL44, L10-19).

It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Matsumura et al.** with the method of **Swoboda et al.** that included determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the actual test environment; and determining, in the virtual test environment, an indication of a signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used, so that would allow evaluating the integrity of the input test signal and a resulting output signal from the virtual device based on the determined indication of the signal transmission time of the actual electronic device in the actual test environment and the determined indication of the signal transmission time of the actual electronic device in the environment the actual electronic device might ordinarily be used. The artisan would have been motivated because that would allow simulating the operation of the target chip and key peripheral features including the timers and serial port

when the target chip includes them in a cost-effective manner; allow simulating the target device even when the rest of the circuitry for the target board was incomplete; and would allow simulating the target board and the target device, so that software development for the device could be performed by one group of engineers while another group of engineers was designing as yet unfinished target device and system.

Conclusion

ACTION IS FINAL

9. Applicant's amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 14, 2005

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER